What is claimed is :

1. A semiconductor packaging structure comprising:

an electrically substrate having a top surface and a bottom surface;

a semiconductor die uplying said top surface;

a first array comprising a first plurality of solder joints, mounted on said die surface and projecting downwardly;

a second array comprising a second plurality of solder joints, mounted on said top surface, integral with said first array, therefrom, connecting said die surface and said top surface, and said solder joint of said second array comprising a flat surface at its front edge; and

a group of solder paste located between said first array and said second array, therefrom, said first plurality of solder joints and said second plurality of solder joints having a higher melting point than said solder paste.

2. The structure described in claim 1 wherein said first array integral with said second array, at integral process, predetermined the shape of solder joints, said first plurality of solder joints and said second plurality of solder joints were not melted, and said solder paste were melted.

3. The structure described in claim 1 further comprising:

a print circuit board underlying said substrate;

a third array comprising a third plurality of solder joints, mounted on said

bottom surface and projecting downwardly;

a fourth array comprising a fourth plurality of solder joints, mounted on said print circuit board, integral with said third array, therefrom, connecting said bottom surface and print circuit board, and said solder joint of said fourth array comprising said flat surface at its front edge; and

a group of solder paste located between said third array and said fourth array, therefrom, said third plurality of solder joints and said fourth plurality of solder joints having a higher melting point than said solder paste.

4. The structure described in claim 3 wherein said third array integral with said fourth array, at integral process, predetermined the shape of solder joints, said third plurality of solder joints and said fourth plurality of solder joints were not melted, and said solder paste were melted.

5. The structure described in claim 1 wherein said solder joint located on said first array comprises said flat surface at its front edge.

6. The structure described in claim 1 wherein said solder joint located on said third array comprises said flat surface at its front edge.

7. The structure described in claim 1 wherein said flat surface of said second plurality of solder joints comprises a concave middle.

8. The structure described in claim 1 wherein said flat surface of said fourth

plurality of solder joints comprises a concave middle.

9. The structure described in claim 1 wherein said flat surface implemented on said first plurality of solder joints is 3% to 80% smaller than said flat surface implemented on said second plurality of solder joints.

10. The structure described in claim 1 wherein said flat surface implemented on said third plurality of solder joints is 3% to 80% smaller than said flat surface implemented on said fourth plurality of solder joints.

11. The structure described in claim 1 wherein said semiconductor package had been assembled, said first plurality of solder joints and said second plurality of solder joints were not melted, and said solder paste were melted.

12. The structure described in claim 1 wherein said semiconductor package had been assembled, said third plurality of solder joints and said fourth plurality of solder joints were not melted, and said solder paste were melted.

13. The structure described in claim 1 wherein said first plurality of solder joints and said second plurality of solder joints having a higher or equal melting point than said fourth plurality of solder joints.

14. The structure described in claim 1 wherein said first plurality of solder joints and said second plurality of solder joints having a higher or equal melting point than said third plurality of solder joints.

15. The structure described in claim 1 wherein the number of semiconductor dies is at least two.

16. The structure described in claim 1 wherein said solder joints implemented on said die surface are heading in correspondence with said solder joints implemented on said top surface.

17. The structure described in claim 1 wherein said solder joints implemented on said bottom surface are heading in correspondence with said solder joints implemented on said print circuit board.

18. A semiconductor packaging structure comprising:

at lease one semiconductor die;

a print circuit board underlying said dies;

a first array comprising said first plurality of solder joints, mounted on said die surface and projecting downwardly;

a fourth array comprising said fourth plurality of solder joints, mounted on said print circuit board, integral with said first array, therefrom, connecting said die surface and said print circuit board; and

a group of solder paste located between said first array and said and said fourth array, therefrom, said first plurality of solder joints and said fourth plurality of solder joints having a higher melting point than said solder paste.

19. The structure described in claim 18 wherein said first array integral with said fourth array, at integral process, predetermined the shape of solder joints, said first plurality of solder joints and said fourth plurality of solder joints were not melted, and said solder paste were melted.